**IN THE UNITED STATES PATENT TRADEMARK OFFICE**

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| **Applicant** | **WESTON, LANCE** |
| **Application Number** | **10/750,385** |
| **Confirmation Number** | **8983** |
| **Filing Date** | **12/31/2003** |
| **Title** | **INPUT TRANSIENT PROTECTION FOR ELECTRONIC DEVICES** |
| **Docket Number** | **H0006069-0555** |
| **Examiner** | **DINH, TUAN T** |
| **Art Unit** | **2841** |

## REVISED APPEAL BRIEF ON BEHALF OF LANCE WESTON

This is an Appeal from the Final Rejection of Claims 62-70 and 76-84 by the Office Action of 12/28/2007. This revised brief is submitted in response to the notice of non-compliant appeal brief dated 10/23/2008.

### REAL PARTY IN INTEREST

The real parties in interest are the inventors Lance Weston, Edward L. Fontana and Larry A. Sternstein and Honeywell International Inc.

### II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

### III. STATUS OF THE CLAIMS

*CERTIFICATE OF TRANSMISSION*
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*Appeal Related Matters**
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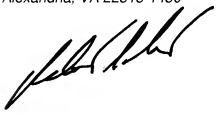

*Registration No. 24,681*

A) Claims 1-12 and 27-89 are pending in the application.
B) Claims 1-12 and 27-61 are withdrawn.
C) Claims 71-75 and 85-89 are allowed
D) Claims 62-70, 76-84 are rejected.
E) Claims 62-70, 76-84 are on appeal.

**IV. STATUS OF AMENDMENTS**

An after final response under 37 C.F.R. § 1.116 was filed on 03/10/2008. That response did not amend the claims. The advisory action of *04/09/2008* states that for the purposes of appeal the amendment would not be entered and the response did not place the application in condition for allowance.

**V. SUMMARY OF CLAIMED SUBJECT MATTER**

The pending claims are for a circuit protection system and relates to electronic circuit boards and particularly passive means for protecting against voltage transient in electronic components. Alarm systems and many other electronic devices are attached through wires to external devices. These wires are subject to voltage transients that can lead to failure of individual components on the circuit board. The problem is particularly acute with respect to resistors at an input for a given electronic circuit. Wires that are connected to the input for the circuit, referred to as "external wires" have voltage transients in them. The usual failure mode of such resistors is a changing value of the resistor as the transient arcs from the body of the resistor, burning off the film deposited on the resistor.

A circuit board assembly which includes an electrically insulating layer, a conductive printed wiring layer formed on the surface of the electrically insulating layer and includes a plurality of conductive paths, a conductive trace on the electrically insulating layer and apparatus for dissipating a transient in addition to a surface mount resistor fixed in relation to the trace. In some forms of the

invention the surface mount resistor has opposed generally planar lips. The trace may also be generally planar. In some cases the lower 10 lips and the trace are generally parallel. The generally planar lips of the surface mount resistor may be closer to the trace than the thickness of the surface mount resistor. A single geometric plane may extend through substantially all of the lips and all of the trace. In some cases the lower surface of the lips and the lower surface of the trace are substantially coplanar. In some cases the upper surface of the lower lip and the upper surface of the trace are substantially coplanar. In other cases the lower surface of the lower lip and the lower surface of the trace are substantially coplanar and in addition the upper surface of the lip and the upper surface of the trace are substantially coplanar.

The claims will be better understood by reference to a portion of Fig. 2 that illustrates a typical surface mount resistor: As described in the specification on page 7, the typical surface mount resistor has industry standard U-shaped end caps 2, 4. It will be understood that the end cap 4 is identical to end cap 2. For the purpose of illustrating the internal structure the end cap 2 has been cut away solely for the purpose of illustration.

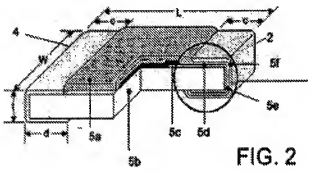

FIG. 2

The independent claims which are involved in this appeal are claims 62, 66, 76 and 80 are reproduced below followed immediately by Fig. 1 (marked up with bold font legends to emphasize 4 discrete edges as well as other features of the structure).

Reference numerals and comments are added to these claims in bold font parenthetical statements to improve clarity.

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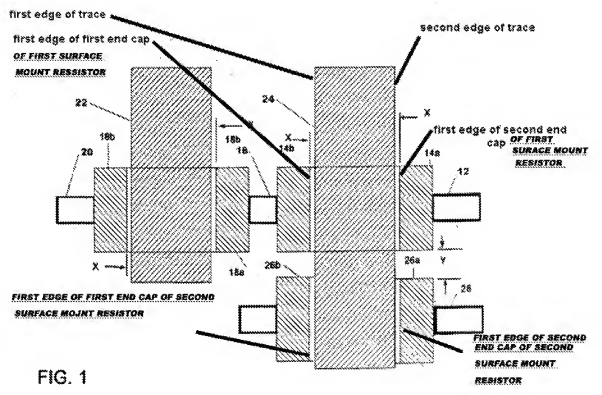


FIG. 1

62. A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board **(50 in Fig. 3; specification p. 7 line 16)**

a surface mount component (14 in Fig. 2 specification p. 8, line1) mounted on said printed circuit board, said surface component having first and second end caps, **(2, 4 in Fig 2 specification p. 7 line 22; 14a, 14b in Fig. 1 specification p. 8, line7)** said first and second end caps each having a first edge**; (expressly marked as 'first edge of first end cap" and (first edge of second end cap" specification p. 10, line 26, p. 5, lines16, 19; p. 9, line 24)** a conductive trace **(24 specification p. 8, line 8; p. 5. lines 33-34)** on said printed circuit board having first and second

opposed edges **(expressly marked as 'first edge of trace" and ;"second edge of trace")** extending intermediate said first and second end caps, **(2, 4 in Fig 2 specification p. 7 line 22, 14a, 14b in Fig. 1 specification p. 8, line7; p. 5. lines 33-34)** said first and second opposed edges **(expressly marked as 'first edge of first trace" and ;"second edge of trace")** being coplanar **(Fig. 1 and specification p. 9, lines 17-19; p.6, lines 20-26)** and thereby defining a plane, said plane intersecting said first edge of said first end cap **(expressly marked as 'first edge of first end cap" specification p. 10, line 26, p. 5, lines16, 19; p. 9, line 24))** and intersecting said first edge of said second end cap, **(expressly marked as;"first edge of second end cap")** said first edge of said trace **(expressly marked as 'first edge of trace")** being disposed in parallel spaced relation to said first edge of said first end cap **(expressly marked as 'first edge of first end cap")** and said second edge of said trace **(expressly marked as "second edge of trace")** being disposed in parallel spaced relation to said first edge of said second end cap. **(expressly marked as;"first edge of second end cap")**

66. A circuit protection system **(60 Specification P. 7, Line 16)** for dissipating transients without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board; **(50 in Fig. 3; specification p. 7 line 16)**

a first surface mount component **(14 in Fig. 2 specification p. 8, line1)** mounted on said printed circuit board, said surface component having first and second end caps, **(2, 4 in Fig 2 specification p. 7 line 22; 14a, 14b in Fig. 1 specification p. 8, line7)**said first and second end caps each having a first edge; **expressly marked as 'first edge of first end cap" and (first edge of second end cap" specification p. 10, line 26, p. 5, lines16, 19; p. 9, line 24)**

a second surface mount component **(26 in Fig. 2 specification p. 8, line1)** mounted on said printed circuit board, **(50 in Fig. 3; specification p. 7 line 16)** said surface component having first and second end caps, said first and second end caps **(2, 4 in**

**Fig 2 specification p. 7 line 22; 14a, 14b in Fig. 1 specification p. 8, line7)** each having a first edge;**(the first edge of the first and second end caps of the second component correspond to the positions of the first edge of the first and second end caps of the first component which have been expressly marked herein)**

a conductive trace **(24 specification p. 8, line 8; p. 5. lines 33-34)** on said printed circuit board **(50 in Fig. 3; specification p. 7 line 16)** having first and second opposed edges **(expressly marked as 'first edge of trace" and ;"second edge of trace")** extending intermediate said first and second end caps **(2, 4 in Fig 2 specification p. 7 line 22; 14a, 14b in Fig. 1 specification p. 8, line7)** of said first surface mounted component, **(14 in Fig. 2 specification p. 8, line1)** said first and second opposed edges being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap **(expressly marked as 'first edge of first end cap" specification p. 10, line 26, p. 5, lines16, 19; p. 9, line 24)** of said first surface mounted component and intersecting said first edge of said second end cap **(expressly marked as;"first edge of second end cap")** of said first surface mounted component, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap of said first surface mounted component and said second edge of said trace is disposed in parallel spaced relation to said first edge of said second end cap of said first surface mounted component; and

said conductive trace **(24 specification p. 8, line 8; p. 5. lines 33-34)** on said printed circuit board **(50 in Fig. 3; specification p. 7 line 16)** having said first and second opposed edges **(expressly marked as 'first edge of trace" and ;"second edge of trace")** extending intermediate said first and second end caps of said second surface mounted component, **(26 in Fig. 2 specification p. 8, line1)** said plane intersecting said first edge of said first end cap **(2 in Fig 2 specification p. 7 line 22, 14a, 14b in Fig. 1 specification p. 8, line7; p. 5. lines 33-34)** of said second surface mounted component and intersecting said first edge of said second end cap **(4 in Fig 2 specification p. 7 line 22, 14a, 14b in Fig. 1 specification p. 8, line7; p. 5. lines**

**33-34)** of said second surface mounted component, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap of said second surface mounted component and said second edge of said trace being disposed in parallel spaced relation to said first edge of said second end cap of said second surface mounted component. **(26 in Fig. 2 specification p. 8, line1)**

76. A circuit protection system for dissipating transients
without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board **(50 in Fig. 3; specification p. 7 line 16)**;

a surface mount resistor mounted **(2, 4 in Fig 2 specification p. 7 line 22; 14a, 14b in Fig. 1 specification p. 8, line7)**on said printed circuit board, said surface resistor having first and second end caps, **(2, 4 in Fig 2, specification p. 7 line 22; 14a; 14a, 14b in Fig. 1 specification p. 8, line7)** said first and second end caps **(2, 4 in Fig 2, specification p. 7 line 22; 14a; 14a, 14b in Fig. 1 specification p. 8, line7)** each having a first edge **(see marked Fig. 1 <u>above</u> captions identifying each first edge)**;

a conductive trace **(24 specification p. 8, line 8; p. 5. lines 33-34)** on said printed circuit board having first and second opposed edges **(expressly marked as 'first edge of trace" and ;"second edge of trace" in marked Fig. 1 <u>above</u> and inherent in specification p. 10, lines 25-28 reference to bands that the bands have edges particularly where the drawing shows a band with edges)** extending intermediate said first and second end caps, **(2, 4 in Fig 2, 14a, 14b in Fig. 1 in drawing and inherent in specification p. 10, lines 25-28 reference to bands that the bands have edges particularly where the drawing shows a band with edges)** said first and second opposed edges **(expressly marked as 'first edge of trace" and ;"second edge of trace" in marked Fig. 1 and inherent in specification p. 10, lines 25-28 reference to bands that the bands have edges particularly where the drawing shows a band with edges)** being coplanar and thereby defining a plane,

said plane intersecting said first edge of said first end cap **(expressly marked as 'first edge of first end cap" in in marked Fig. 1 and inherent in specification p. 10, lines 25-28 reference to bands that the bands have edges particularly where the drawing shows a band with edges)** and intersecting said first edge of said second end cap, . **(expressly marked as;"first edge of second end cap" in in marked Fig. 1 and inherent in specification p. 10, lines 25-28 reference to bands that the bands have edges particularly where the drawing shows a band with edges)** said first edge of said trace **(expressly marked as 'first edge of first trace" in in marked Fig. 1 and inherent in specification p. 10, lines 25-28 reference to bands that the bands have edges particularly where the drawing shows a band with edges)** being disposed in parallel spaced relation to said first edge of said first end cap **(expressly marked as 'first edge of first end cap" in in marked Fig. 1 and inherent in specification p. 10, lines 25-28 reference to bands that the bands have edges particularly where the drawing shows a band with edges)** and said second edge of said trace **(expressly marked as "second edge of trace" in in marked Fig. 1 and inherent in specification p. 10, lines 25-28 reference to bands that the bands have edges particularly where the drawing shows a band with edges)** being disposed in parallel spaced relation to said first edge of said second end cap. . **(expressly marked as;"first edge of second end cap" in marked Fig. 1 and inherent in specification p. 10, lines 25-28 describing an embodiment that has a single band that extends close to opposed edges of respective end caps.)**

80. (Previously presented) A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board**(50 in Fig. 3; specification p. 7 line 16)**;

a first surface mount resistor **(14 specification p. 8 line 1; having end caps 14a, 14b Fig. 1 specification p. 8, line7)** mounted on said printed circuit board **50**, said surface resistor having first and second end caps**(2, 4 in Fig 2, specification p. 7**

**line 22; 14a; 14a, 14b in Fig. 1 specification p. 8, line7)** , said first and second end caps each having a first edge **(see marked Fig. 1)**;

a second surface mount resistor (**26 specification p. 8 line 1, Fig. 1 shows the end caps thereof 26a, 26b, specification p. 8, line 11; description of first surtace mount resistor applies *mutatis mutandis* to second surface mount resistor);** mounted on said printed circuit board **50**, said surface resistor having first and second end caps (**Fig. 1 shows the end caps thereof 26a, 26b, specification p. 8, line 11**), said first and second end caps each having a first edge **(expressly marked as 'first edge of first end cap" and (first edge of second end cap" specification p. 10, line 26, p. 5, lines16, 19; p. 9, line 24)**;

a conductive trace **(24 specification p. 8, line 8; p. 5. lines 33-34)** on said printed circuit board **50** having first and second opposed edges **(inherent that a trace has edges an expressly marked as 'first edge of trace" and "second edge of trace" in marked drawing)** extending intermediate said first and second end caps **(14a, 14b Fig. 1 specification p. 8, line7)** of said first surface mounted resistor **(14 specification p. 8 line 1; having end caps 14a, 14b Fig. 1 specification p. 8, line7)**, said first and second opposed edges **(inherent that a trace has edges an expressly marked as 'first edge of trace" and ;"second edge of trace" in marked drawing)** being coplanar **(Fig. 1 and specification p. 9, lines 17-19; p.6, lines 20-26)** and thereby defining a plane, said plane intersecting said first edge of said first end cap of said first surface mounted resistor **(expressly marked as 'first edge of first end cap" specification p. 10, line 26, p. 5, lines16, 19; p. 9, line 24))** and intersecting said first edge of said second end cap **(expressly marked as;"first edge of second end cap")** of said first surface mounted resistor, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap of said first surface mounted resistor **(expressly marked as 'first edge of first end cap")** and said second edge of said trace is disposed in parallel spaced relation to said first edge of said second end cap of said first surface mounted resistor **(expressly marked as;"first edge of second end cap")**; and

said conductive trace **(24 specification p. 8, line 8; p. 5. lines 33-34)** on said printed circuit board **50** having said first and second opposed edges **(inherent that a trace has edges an expressly marked as 'first edge of trace" and "second edge of trace" in marked drawing)** extending intermediate said first and second end caps **(26a 26b specification p. 8, line 11 Figure 1**) of said second surface mounted resistor, said plane intersecting said first edge **(marked Fig. 1)** of said first end cap of said second surface mounted resistor **26** and intersecting said first edge of said second end cap **(see marked Fig. 1)** of said second surface mounted resistor **(see marked Fig. 1)**, said first edge **(see marked Fig. 1)** of said trace **(see marked Fig. 1)** being disposed in parallel spaced relation to said first edge **(see marked Fig. 1)** of said first end cap **( 26a, see marked Fig. 1)** of said second surface mounted resistor **26** and said second edge of said trace **24** being disposed in parallel spaced relation to said first edge **(see marked Fig. 1)** of said second end cap **(26b, see marked Fig. 1)** of said second surface mounted resistor **(26, see marked Fig. 1)**.

**VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

A. Whether or not Claims 63, 67, 72, 77, 81, and- 86 are incomplete under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim-the subject matter which applicant regards as the invention..

B. Whether or not Claims 62-70, 76-84 are patentable under 35 U.S.C. §102(e) as being anticipated by Devoe (U.S. Patent 6,690,558)

**VII. ARGUMENT**

**A. Whether or not Claims 63, 67, 72, 77, 81, and- 86 are incomplete under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim-the subject matter which applicant regards as the invention.**

The rejection includes:

> "Claims 63, 67, 72, 77, 81, and 86 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim-the subject matter which applicant regards as the invention.
>
> Regarding claim 63, lies 2-4 is unclear. What does applicant mean of "second edge of the trace and first edge of the second cap are both substantially equal to X"? Does applicant mean either the dimension or size of the second edge of the trace and -the first edge of the second cap are both substantially equal to X (0.1 in).
>
> Rejected claims 67, 72, 77, and 88 are similar to claim 63.
>
> Please clarify."

Addressing this issue inherently requires duplication of the preceding section entitled V. SUMMARY OF CLAIMED SUBJECT MATTER. To avoid any assertion that Appellant has not responded, the following comments expressly directed to the rejection are provided. The following make express reference to the same marked Fig. 1 that appears on Page 6 of this document.

The issue raised by the Examiner seeks the meaning of a claim phrase. It is submitted that the language quoted is already clear when considered in the context in which it appears particularly by referring to Figure 1 of the drawing.

The entire claim 63 is:

> 63. The circuit protection system as described in claim 62 wherein **the dimension of the space intermediate**

(1) said first edge of said trace and said first edge of said first end cap and
(2) said second edge of said trace and said first edge of said second end cap
**are both substantially equal to X. (emphasis added)**

The marked up copy of Fig. 1 of the drawing above emphasizes that which is shown in the drawing including the explicitly labeled dimensions. It will be understood that "X" is used to refer the dimension of the space intermediate both a first set of two edges as well as the dimension of the space intermediate a second set of two edges.

The term "X" is used in the same sense that it is used in elementary algebra. See
http://www.newton.dep.anl.gov/askasci/math99/math99228.htm
http://www.garlikov.com/math/UnderstandingAlgebra.html

As used in claim 63 the dimension is an unspecified quantity, however, the claims make clear that both of the respective dimensions are substantially equal to X. Thus, the first and second dimensions are inherently substantially equal to each other. The use of the standard algebraic representation in claim 63 facilitates subsequent more specific claims. Claim 63 further limits claim 62 because it specifies that two specific dimensions are substantially equal. Claim 65 is a more specific claim that specifies that the two recited dimensions are both substantially equal to each other and substantially equal to .01 inch.

It is respectfully submitted that the asserted issue relates to specific words out of the context in which they appear. The words when taken in context are fully supported by both the original specification and the specification as amended in the response dated 10/11/06.

The meaning of the words is most apparent by consideration of page 8 of the specification.

It is noted that a search of USPTO records for the string "is equal to X" produces

the following:

> **"Results of Search in US Patent Collection db for:**
> **"is equal X"":** 3192 patents.
> *Hits **1** through **50** out of **3192** "*

Obviously, similar searches for other Latin or Greek alphabet letters would identify many more additional hits and establish the use of such terminology is usual and customary. Other variations such as "is equal to X" or "equals X" iterated for other symbols would provide even more abundant examples.

The preceding applies *mutatis mutandis* to the other claims 67, 72, 77, 81, and 86 rejected under 35 U.S.C. 112, second paragraph. Some of these claims are directed to embodiments that include more than one surface mount component.

**B. Whether or not Claims 62-70, 76-84 are patentable under 35 U.S.C. §102(e) as being anticipated by Devoe (U.S. Patent 6,690,558)**

The rejection is:

> 5. Claims 62-70,76-84 are rejected under 35 U.S.C. 102(e) as being anticipated by Devoe (U.S. Patent 6,690,558)
>
> As to claims 62, 76, Devoe discloses a high power resistor device (30; 40) as shown in figures 3A-3C comprising:
>
> a printed circuit board (48, column 4, line 24) having a SMT component (30; 40) mounted on, the component (30; 40) having first and second end caps (14), and each caps having a first edge;
>
> a conductive trace (46, see figure 3C) formed on the PCB (48) having first and second opposed edges extending intermediate said first and second caps (14), the edges of the trace (46) being defined a plane, see figure 3C and intersecting the first edge of the first cap (14) and intersecting the first edge of the second cap (14), the edge of the trace (46) disposed in parallel spaced relative to the edge of the first and second caps respectively.
>
> As to claims 66,80, Devoe discloses a high power resistor device (30; 40) as shown in figures 3A-3C comprising:

a printed circuit board (48, column 4, line 24) having first and second SMT components (30,40) mounted on, the components (30, 40) having first and second end caps (14), and each caps having a first edge;
a conductive trace (46, see figure 3C) formed on the PCB (48) having first and second opposed edges extending intermediate said first and second caps (14), the edges of the trace (46) being defined a plane, see figure 3C and intersecting the first edge of the first cap (14) and intersecting the first edge of the second cap (14), the edge of the trace (46) disposed in parallel spaced relative to the edge of the first and second caps respectively, and said plane intersecting said first edge of said first end cap of said second surface mounted component (40) and intersecting said first edge of said second end cap of said second surface mounted component, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap of said second surface mounted component and said second edge of said trace being disposed in parallel spaced (sic)

Regarding claims 63-65, 67-70, 77-79, and 81-84, Devoe discloses the second edge of the trace being substantially the same to the first edge of the second cap.

Each independent claim in the rejected claims includes the following:

"...**a conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps, said first and second opposed edges being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap and intersecting said first edge of said second end cap, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap and said second edge of said trace being disposed in parallel spaced relation to said first edge of said second end cap** ..." (emphasis added)

The following is a marked copy of Devoe Fig, 3C in which a bold horizontal line represents the plane defined by the edges of the two discrete traces 46, 46.

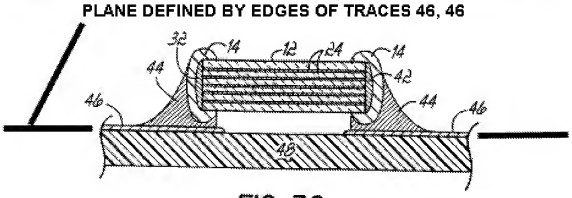


FIG. 3C

No part of either trace 46, 46 in Devoe is coplanar with any part of either end cap 14, 14. A plane defined by the edges of either or both traces 46, 46 does not intersect the end caps 14, 14. Neither trace 46 extends intermediate end caps 14, 14 Instead, the traces 46, 46 extends in a plane at a lower elevation as expressly shown by the bold horizontal line in the above Fig. 3C and marked as "PLANE DEFINED BY EDGES OF TRACES 46, 46".. Thus, the reference does not have the same structure. In addition the traces 46, 46 are attached to the end caps by solder 44 and thus does not have a spacing that is necessary for the function of present invention as well as the explicit, specific spacing recited in the claims. Furthermore, the trace in Devoe is used to connect the device to the board. Any surge will inherently pass through that trace. Thus, the traces 46, 46 in Devoe are the source of transients not a protection from transients!

The above is summarized in the following table:

| **THE PARSED CLAIM with reference numerals added** | **THE REFERENCE** | **COMMENT** |
|---|---|---|
| 62. A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which | | |

| | | |
|---|---|---|
| comprises: | | |
| a printed circuit board; | | |
| a surface mount component mounted on said printed circuit board, said surface component having first and second end caps, said first and second end caps each having a first edge; | | |
| a conductive trace 24 on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps, | The rejection asserts element 46 of the reference meets the claim. | Element 46 of the reference is **not intermediate** the end caps 14, 14 of the reference3,. The specification of the reference makes clear at column 4, lines 3-4 that the respective end caps of the 14, 14 of the resistor 32 are joined to respective traces (plural not singular) on the substrate 48. The reference has **no trace intermediate the end caps.** |
| said first and second opposed edges being coplanar and thereby defining a plane, | The elements 46, 46 do have edges that could define a plane | |
| said plane intersecting said first edge of said first end cap and intersecting said first edge of said second end cap, | | A **plane** defined by the elements 46, 46 **does not intersect any part of any end cap 14** |
| said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap and said second edge of said trace being disposed in parallel | | The respective traces are physically and electrically connected to the end caps! Thus, they **clearly are not disposed in spaced relation much less in parallel spaced** |

| | | |
|---|---|---|
| spaced relation to said first edge of said second end cap. | | **relation to the end caps.** |

Thus, the reference does not have the structure explicitly claimed, does not have either intentionally or implicitly include the purpose of the invention, and does not achieve the result of the present invention either intentionally or inherently. Accordingly, there is no rational, good faith, plausible, or credible support for rejection based on the cited reference under 35 U.S.C. §102(e) or any other part of 35 U.S.C. §102 or §103.

Accordingly, it is requested that the Board reverse the Examiner.

Respectfully submitted,

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**(VII) CLAIMS APPENDIX**

1. (withdrawn) A circuit board assembly which comprises:

an electrically insulating layer;

a conductive printed wiring layer formed on the surface of said electrically insulating layer and including a plurality of conductive paths;

a conductive trace on said electrically insulating layer and means for dissipating a transient;

a surface mount resistor fixed in relation to said trace.

2. (withdrawn) The circuit board assembly as described in claim 1 wherein said surface mount resistor has opposed generally planar lips.

3. (withdrawn) The circuit board assembly as described in claim 1 wherein said surface mount resistor has a generally planar lips and said trace is also generally planar.

4. (withdrawn) The circuit board assembly as described in claim 1 wherein said surface mount resistor has a generally planar lower lip, said trace is also generally planar and said lower lip and said trace are generally parallel.

5. (withdrawn) The circuit board assembly as described in claim 2 wherein said generally planar lips of said surface mount resistor are closer to said trace than the thickness of said surface mount resistor.

6. (withdrawn) The circuit board assembly as described in claim 2 wherein said lips and said trace are parallel.

7. (withdrawn) The circuit board assembly as described in claim 4 wherein a single geometric plane extends through substantially all of said lips and all of said trace.

8. (withdrawn) A circuit board assembly as described in claim 7 wherein the lower surface of said lips and the lower surface of said trace are substantially coplanar.

9. (withdrawn) A circuit board assembly as described in claim 7 wherein the upper surface of said lower lip and the upper surface of said trace are substantially coplanar.

10. (withdrawn) A circuit board assembly as described in claim 7 wherein the lower surface of said lower lip and the lower surface of said trace are substantially coplanar and in addition the upper surface of said lip and the upper surface of said trace are substantially coplanar.

11. (withdrawn) A circuit board assembly as described in claim 10 wherein said surface mount resistor has a height of t and the spacing between said lip and said trace is less than t.

12. (withdrawn) A circuit board assembly as described in claim 11 wherein the spacing between said lip and said trace is no more than one half t.

Claims 13-26 (cancelled)

27. (withdrawn) A circuit board assembly which comprises:

an electrically insulating layer;

a conductive printed wiring layer formed on the surface of said electrically insulating layer and including a plurality of conductive paths;

a conductive trace on said electrically insulating layer and means for dissipating a transient;

a first surface mount resistor fixed in closely spaced relation to said trace;

a second surface mount resistor fixed in closely space relation to said trace.

28. (withdrawn) The circuit board assembly as described in claim 27 wherein each of said surface mount resistors has opposed generally planar lips.

29. (withdrawn) The circuit board assembly as described in claim 27 wherein each of said surface mount resistors has a generally planar lips and said trace is also generally planar.

30. (withdrawn) The circuit board assembly as described in claim 27 wherein each of said surface mount resistors has a generally planar lower lip, said trace is also generally planar and all of said lower lips and said trace are generally parallel.

31. (withdrawn) The circuit board assembly as described in claim 27 wherein said generally planar lips of said surface mount resistors are closer to said trace than the thickness of said surface mount resistors.

32. (withdrawn) The circuit board assembly as described in claim 28 wherein said lips and said trace are parallel.

33. (withdrawn) The circuit board assembly as described in claim 32 wherein a single geometric plane extends through substantially all of said lips and all of said trace.

34. (withdrawn) A circuit board assembly as described in claim 33 wherein the lower surface of said lips and the lower surface of said trace are substantially coplanar.

35. (withdrawn) A circuit board assembly as described in claim 33 wherein the upper surface of said lower lips and the upper surface of said trace are substantially coplanar.

36. (withdrawn) A circuit board assembly as described in claim 33 wherein the lower surface of said lower lips and the lower surface of said trace are substantially coplanar and in addition the upper surface of said lips and the upper surface of said trace are substantially coplanar.

37. (withdrawn) A circuit board assembly as described in claim 33 wherein said surface mount resistor has a height of t and the spacing between each of said lips and said trace is less than t.

38. (withdrawn) A circuit board assembly as described in claim 37 wherein the spacing between each of said lips and said trace is no more than one half t.

39. (withdrawn) A circuit board assembly as described in claim 27 wherein the distance between said first and second resistors is greater than the height of each resistor.

40. (withdrawn) A circuit board assembly as described in claim 28 wherein the distance between said first and second resistors is greater than the height of each resistor.

41. (withdrawn) A circuit board assembly as described in claim 29 wherein the distance between said first and second resistors is greater than the height of each resistor.

42. (withdrawn) A circuit board assembly as described in claim 30 wherein the distance between said first and second resistors is greater than the height of each resistor.

43. (withdrawn) A circuit board assembly as described in claim 31 wherein the distance between said first and second resistors is greater than the height of each resistor.

44. (withdrawn) A circuit board assembly as described in claim 32 wherein the distance between said first and second resistors is greater than the height of each resistor.

45. (withdrawn) A circuit board assembly as described in claim 33 wherein the distance between said first and second resistors is greater than the height of each resistor.

46. (withdrawn) A circuit board assembly as described in claim 34 wherein the distance between said first and second resistors is greater than the height of each resistor.

47. (withdrawn) A circuit board assembly as described in claim 35 wherein the distance between said first and second resistors is greater than the height of each resistor.

48. (withdrawn) A circuit board assembly as described in claim 36 wherein the distance between said first and second resistors is greater than the height of each resistor.

49. (withdrawn) A circuit board assembly as described in claim 38 wherein the distance between said first and second resistors is greater than the height of each resistor.

50. (withdrawn) A circuit board assembly as described in claim 27 wherein the distance between said first and second resistors is at least three times the height of each resistor.

51. (withdrawn) A circuit board assembly as described in claim 28 wherein the distance between said first and second resistors is at least three times the height of each resistor.

52. (withdrawn) A circuit board assembly as described in claim 29 wherein the distance between said first and second resistors is at least three times the height of each resistor.

53. (withdrawn) A circuit board assembly as described in claim 30 wherein the distance between said first and second resistors is at least three times the height of each resistor.

54. (withdrawn) A circuit board assembly as described in claim 32 one wherein the distance between said first and second resistors is at least three times the height of each resistor.

55. (withdrawn) A circuit board assembly as described in claim 32 wherein the distance between said first and second resistors is at least three times the height of each resistor.

56. (withdrawn) A circuit board assembly as described in claim 33 wherein the distance between said first and second resistors is at least three times the height of each resistor.

57. (withdrawn) A circuit board assembly as described in claim 34 wherein the distance between said first and second resistors is at least three times the height of each resistor.

58. (withdrawn) A circuit board assembly as described in claim 35 wherein the distance between said first and second resistors is at least three times the height of each resistor.

60. (withdrawn) A circuit board assembly as described in claim 37 wherein the distance between said first and second resistors is at least three times the height of each resistor.

60. (withdrawn) A circuit board assembly as described in claim 38 wherein the distance between said first and second resistors is at least three times the height of each resistor.

61. (withdrawn) A circuit board assembly as described in claim 39 wherein the distance between said first and second resistors is at least three times the height of each resistor.

62. (Rejected) A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board;

a surface mount component mounted on said printed circuit board, said surface component having first and second end caps, said first and second end caps each having a first edge;

a conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps, said first and second

opposed edges being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap and intersecting said first edge of said second end cap, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap and said second edge of said trace being disposed in parallel spaced relation to said first edge of said second end cap.

63. (Rejected) The circuit protection system as described in claim 62 wherein the dimension of the space intermediate
(1) said first edge of said trace and said first edge of said first end cap and
(2) said second edge of said trace and said first edge of said second end cap
are both substantially equal to X.

64. (Rejected) The circuit protection system as described in claim 63 wherein said surface mount component has a height dimension t and X is less than t.

65. (Rejected) The circuit protection system as described in claim 63 wherein X is approximately .01 inch.

66. (Rejected) A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board;

a first surface mount component mounted on said printed circuit board, said surface component having first and second end caps, said first and second end caps each having a first edge;

a second surface mount component mounted on said printed circuit board, said surface component having first and second end caps, said first and second end caps each having a first edge;

a conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps of said first surface mounted component, said first and second opposed edges being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap of said first surface mounted component and intersecting said first edge of said second end cap of said first surface mounted component, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap of said first surface mounted component and said second edge of said trace is disposed in parallel spaced relation to said first edge of said second end cap of said first surface mounted component; and

said conductive trace on said printed circuit board having said first and second opposed edges extending intermediate said first and second end caps of said second surface mounted component, said plane intersecting said first edge of said first end cap of said second surface mounted component and intersecting said first edge of said second end cap of said second surface mounted component, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap of said second surface mounted component and said second edge of said trace being disposed in parallel spaced relation to said first edge of said second end cap of said second surface mounted component.

67. (Rejected) The circuit protection system as described in claim 66 wherein dimension of the space intermediate (1) said first edge of said trace and said first edge of said first end cap of said first surface mounted component and (2) said second edge of said trace and said first edge of said second end cap of said first surface mounted component, (3) said first edge of said trace and said first edge of said first end cap of said second surface mounted component and (4) said second edge of said trace and said first edge of said second end cap of said second surface mounted component are all substantially equal to X.

68. (Rejected) The circuit protection system as described in claim 65 wherein said surface mount component has a height dimension t and X is less than t.

69. (Rejected) The circuit protection system as described in claim 67 wherein X is approximately .01 inch.

70. (Rejected) The circuit protection system as described in claim 67 wherein the minimum spacing between the respective end caps of said first and second surface mounted components is at least three times the dimension X.

71. (Allowed) A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board;

a first surface mount component mounted on said printed circuit board, said surface component having first and second end caps, said first and second end caps each having a first edge;

a second surface mount component mounted on said printed circuit board, said surface component having first and second end caps, said first and second end caps each having a first edge;

a first conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps of said first surface mounted component, said first and second opposed edges being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap of said first surface mounted component and intersecting said first edge of said second end cap of said first surface mounted component, said first edge of said first trace being disposed in parallel spaced relation to said first edge of said first end cap of said first surface mounted component and said second edge of said first trace being

disposed in parallel spaced relation to said first edge of said second end cap of said first surface mounted component;

said first conductive trace on said printed circuit board having said first and second opposed edges extending intermediate said first and second end caps of said second surface mounted component, said plane intersecting said first edge of said first end cap of said second surface mounted component and intersecting said first edge of said second end cap of said second surface mounted component, said first edge of said first trace being disposed in parallel spaced relation to said first edge of said first end cap of said second surface mounted component and said second edge of said first trace being disposed in parallel spaced relation to said first edge of said second end cap of said second surface mounted component;

a third surface mount component mounted on said printed circuit board, said third surface component having first and second end caps, said first and second end caps each having a first edge;

a second conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps of said third surface mount component, said first and second opposed edges of said second conductive trace being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap of said third surface mount component and intersecting said first edge of said second end cap of said third surface mount component, said first edge of said second trace being disposed in parallel spaced relation to said first edge of said first end cap of said third surface mount component and said second edge of said second trace being disposed in parallel spaced relation to said first edge of said second end cap of said third surface mount component.

72. (Allowed) The circuit protection system as described in claim 71 wherein dimension of the space intermediate (1) said first edge of said first trace and said first edge of said first end cap of said first surface mounted component, (2) said

second edge of said first trace and said first edge of said second end cap of said first surface mounted component, (3) said first edge of said first trace and said first edge of said first end cap of said second surface mounted component and (4) said second edge of said first trace and said first edge of said second end cap of said second surface mounted component are all equal to X, (5) said first edge of said second trace and said first edge of said first end cap of said third surface mounted component, and (6) said second edge of said second trace and said first edge of said second end cap of said third surface mounted component are all substantially equal to X.

73. (Allowed) The circuit protection system as described in claim 72 wherein each surface mount component has a height dimension t and X is less than t.

74. (Allowed) The circuit protection system as described in claim 72 wherein X is approximately .01 inch.

75. (Allowed) The circuit protection system as described in claim 71 wherein the minimum spacing between the respective end caps of said first and second surface mounted components is at least three times the dimension X.

76. (Rejected) A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board;

a surface mount resistor mounted on said printed circuit board, said surface resistor having first and second end caps, said first and second end caps each having a first edge;

a conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps, said first and second

opposed edges being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap and intersecting said first edge of said second end cap, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap and said second edge of said trace being disposed in parallel spaced relation to said first edge of said second end cap.

77. (Rejected) The circuit protection system as described in claim 76 wherein dimension of the space intermediate (1) said first edge of said trace and said first edge of said first end cap and (2) said second edge of said trace and said first edge of said second end cap are both substantially equal to X.

78. (Rejected) The circuit protection system as described in claim 77 wherein said surface mount resistor has a height dimension t and X is less than t.

79. (Rejected) The circuit protection system as described in claim 78 wherein X is approximately .01 inch.

80. (Rejected) A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board;

a first surface mount resistor mounted on said printed circuit board, said surface resistor having first and second end caps, said first and second end caps each having a first edge;

a second surface mount resistor mounted on said printed circuit board, said surface resistor having first and second end caps, said first and second end caps each having a first edge;

a conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps of said first surface mounted resistor, said first and second opposed edges being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap of said first surface mounted resistor and intersecting said first edge of said second end cap of said first surface mounted resistor, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap of said first surface mounted resistor and said second edge of said trace is disposed in parallel spaced relation to said first edge of said second end cap of said first surface mounted resistor; and

said conductive trace on said printed circuit board having said first and second opposed edges extending intermediate said first and second end caps of said second surface mounted resistor, said plane intersecting said first edge of said first end cap of said second surface mounted resistor and intersecting said first edge of said second end cap of said second surface mounted resistor, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap of said second surface mounted resistor and said second edge of said trace being disposed in parallel spaced relation to said first edge of said second end cap of said second surface mounted resistor.

81. (Rejected) The circuit protection system as described in claim 80 wherein dimension of the space intermediate (1) said first edge of said trace and said first edge of said first end cap of said first surface mounted resistor and (2) said second edge of said trace and said first edge of said second end cap of said first surface mounted resistor, (3) said first edge of said trace and said first edge of said first end cap of said second surface mounted resistor and (4) said second edge of said trace and said first edge of said second end cap of said second surface mounted resistor are all substantially equal to X.

82. (Rejected) The circuit protection system as described in claim 81 wherein said surface mount resistor has a height dimension t and X is less than t.

83. (Rejected) The circuit protection system as described in claim 82 wherein X is approximately .01 inch.

84. (Rejected) The circuit protection system as described in claim 81 wherein the minimum spacing between the respective end caps of said first and second surface mounted resistors is at least three times the dimension X.

85. (Allowed) A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which comprises:

a printed circuit board;

a first surface mount resistor mounted on said printed circuit board, said surface resistor having first and second end caps, said first and second end caps each having a first edge;

a second surface mount resistor mounted on said printed circuit board, said surface resistor having first and second end caps, said first and second end caps each having a first edge;

a first conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps of said first surface mounted resistor, said first and second opposed edges being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap of said first surface mounted resistor and intersecting said first edge of said second end cap of said first surface mounted resistor, said first edge of said first trace being disposed in parallel spaced relation to said first edge of said first end cap of said first surface mounted resistor and said second edge of said first trace being disposed in parallel

spaced relation to said first edge of said second end cap of said first surface mounted resistor;

said first conductive trace on said printed circuit board having said first and second opposed edges extending intermediate said first and second end caps of said second surface mounted resistor, said plane intersecting said first edge of said first end cap of said second surface mounted resistor and intersecting said first edge of said second end cap of said second surface mounted resistor, said first edge of said first trace being disposed in parallel spaced relation to said first edge of said first end cap of said second surface mounted resistor and said second edge of said first trace being disposed in parallel spaced relation to said first edge of said second end cap of said second surface mounted resistor;

a third surface mount resistor mounted on said printed circuit board, said third surface resistor having first and second end caps, said first and second end caps each having a first edge;

a second conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps of said third surface mount resistor, said first and second opposed edges of said second conductive trace being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap of said third surface mount resistor and intersecting said first edge of said second end cap of said third surface mount resistor, said first edge of said second trace being disposed in parallel spaced relation to said first edge of said first end cap of said third surface mount resistor and said second edge of said second trace being disposed in parallel spaced relation to said first edge of said second end cap of said third surface mount resistor.

86. (Allowed) The circuit protection system as described in claim 85 wherein dimension of the space intermediate (1) said first edge of said first trace and said first edge of said first end cap of said first surface mounted resistor, (2) said second

edge of said first trace and said first edge of said second end cap of said first surface mounted resistor, (3) said first edge of said first trace and said first edge of said first end cap of said second surface mounted resistor and (4) said second edge of said first trace and said first edge of said second end cap of said second surface mounted resistor are all equal to X, (5) said first edge of said second trace and said first edge of said first end cap of said third surface mounted resistor, and (6) said second edge of said second trace and said first edge of said second end cap of said third surface mounted resistor are all substantially equal to X.

87. (Allowed) The circuit protection system as described in claim 86 wherein each surface mount resistor has a height dimension t and X is less than t.

88. (Allowed) The circuit protection system as described in claim 86 wherein X is approximately .01 inch.

89. (Allowed) The circuit protection system as described in claim 71 wherein the minimum spacing between the respective end caps of said first and second surface mounted resistors is at least three times the dimension X.

**(IX)** ***Evidence appendix.***

No evidence is being submitted pursuant to 37 CFR 1.130, 1.131, or 1.132 or of any other evidence entered by the examiner and relied upon by appellant in the appeal. Thus a statement setting forth where in the record that evidence was entered in the record by the examiner is not applicable.

## X RELATED PROCEEDING APPENDIX

There are no related Appeals or Interferences.